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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,237	08/23/2001	Dale T. Platteter	D/A0A73	1681
7590	11/30/2004		EXAMINER	
Patrick R. Roche Fay, Sharpe, Fagan Minnich & McKee, LLP 1100 Superior Avenue, 7th Floor Cleveland, OH 44114-2518			CHEN, TSE W	
			ART UNIT	PAPER NUMBER
			2116	
DATE MAILED: 11/30/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,237	PLATTETER ET AL.	
	Examiner Tse Chen	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 September 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-21 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated September 13, 2004.
2. Claims 1-21 are presented for examination.
3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. The following are fact findings for support of all rejections in the instant Office Action.
 - 4.1. Yamanaka discloses a document processing system [master station 1 comprises typewriter 13 for document processing]¹.
 - 4.2. Yamanaka discloses the system comprises a controller [master station 1], including a master clock [17] and logic [CPU 10 and code sending and receiving circuit 18] for generating a discrete clock synchronization interrupt signal [S11; col.7, ll.6-8; being utilized in a synchronization process, S11 is an interrupt signal requiring the receiving station to act on the signal within an acceptable time of tp – col.7, ll.17-20].
 - 4.3. Yamanaka discloses the system comprises a resource [slave station 2], including a slave clock [27] related to operational timing of the resource [the slave station utilizes a slave clock to provide timing functionality to slave station components such as CPU 20 which inherently, requires a local timing input] and circuitry for receiving and processing the discrete clock synchronization interrupt signal [code sensing and receiving circuit 28 and CPU 20; col.3, ll.5-11; col.7, ll.12-17].

4.4. Yamanaka discloses the system comprises a control bus [data transmission path 5], interconnecting the resource and the controller, for distributing the discrete interrupt signal [col.2, ll.25-28; col.4, ll.20-22].

4.5. Yamanaka discloses the resource circuitry includes a processor [CPU 20] for adjusting the slave clock to provide for compatibility with the controller [col.7, ll.42-47].

4.6. Yamanaka discloses the system includes a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and circuitry for receiving and processing the clock synchronization interrupt signal [code sending and receiving circuit 28 and 38, CPU 20 and 30].

4.7. Yamanaka discloses the control bus [data transmission path 5] interconnects each resource with the controller thereby distributing the interrupt signal to each resource [col.2, ll.25-28; col.4, ll.20-22].

4.8. Yamanaka discloses the circuitry in each resource includes a processor [CPU 20 and 30] for adjusting the slave clock associated with the resource to provide for compatibility with the controller [col.7, ll.42-47].

4.9. Yamanaka discloses the system comprises a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and logic for receiving the discrete interrupt signal [code sending and receiving circuit 28 and 38], processing the discrete interrupt signal [CPU 20 and 30], and synchronizing the slave clock with the master clock [col.7, ll.42-47].

¹ Although there are several embodiments, the pertinent reference items generally have the same functionalities and do not contradict one another [col.6, ll.37-41, ll.53-55].

- 4.10. Yamanaka discloses the system comprises electrical wiring [data transmission path 5] interconnecting the resources and the controller for distributing the discrete interrupt signal to the resources [col.2, ll.25-28; col.4, ll.20-22].
- 4.11. Yamanaka discloses the resources include one or more finishing devices [output circuit 24].
- 4.12. Yamanaka discloses the resources include one or more feeding devices [input circuit 25].
- 4.13. Yamanaka discloses a document processing system comprising a plurality of resources [slave stations 2 and 3] [col.7, ll.3-5].
- 4.14. Yamanaka discloses a method of initially synchronizing the slave clock with the master clock [abstract].
- 4.15. Yamanaka discloses the method comprising saving a value of the master clock in the controller [col.7, ll.9-11].
- 4.16. Yamanaka discloses the method comprising generating a discrete clock synchronization interrupt signal in the controller and distributing the discrete interrupt signal to the resource via the control bus [col.7, ll.6-8].
- 4.17. Yamanaka discloses the method comprising receiving the discrete interrupt signal at the resource and saving a first value of the slave clock [col.7, ll.12-17].
- 4.18. Yamanaka teaches the advantage of synchronizing the master and slave clocks within a range of error in order to avoid problems for practical use [col.1, ll.56-59].
- 4.19. Cheung et al., U.S. Patent 5535217, hereinafter Cheung, discloses a system for synchronizing a master and slave clocks [col.1, ll.8-12].

4.20. Cheung discloses the resource circuitry includes a processor [CPU 202] for determining the compatibility of the slave clock with the master clock [FIG.12; col.3, ll.2-5; col.5, ll.45-53].

4.21. Cheung discloses the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [col.4, ll.37-41; set the precision values such as Q and restrict the transmission times appropriately].

4.22. Cheung discloses a method for synchronizing a controller [master or process B] and resource [slave or process A] clocks [col.1, ll.8-12].

4.23. Cheung discloses the method comprising saving a first value [time T] of the slave clock [col.4, ll.6-7].

4.24. Cheung discloses the method comprising sending a message from the resource to the controller via the network to request the value [time U] saved for the master clock [col.2, ll.66-67; col.4, ll.8-10].

4.25. Cheung discloses the method comprising sending the value saved for the master clock from the controller to the resource via the network [col.2, l.67 to col.3, l.2; col.4, ll.11-12].

4.26. Cheung discloses the method comprising receiving the value saved for the master clock at the resource [col.2, l.2; col.4, l.12].

4.27. Cheung discloses the method comprising saving a second value of the slave clock [time V] in the resource [col.2, ll.2-3; col.4, ll.13-14].

4.28. Cheung discloses the method comprising subtracting the first value [time T] from the second value [time V] to determine a slave clock difference value [V-T] [col.4, ll.30-32].

4.29. Cheung discloses the method comprising adding the difference value [V-T] to the value saved for the master clock [U] to determine a synchronized value for [U+V-T] the slave clock and setting the slave clock to the synchronized value [col.4, ll.37-41; Q=0].

4.30. Cheung discloses the method comprising subtracting the value saved for the slave clock [time T] from the value saved for the master clock [time U] to determine an error value between the slave clock and the master clock [U-T] and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock [col.4, ll.37-41; utilize V and Q in algorithm].

4.31. Cheung discloses the method wherein the periodic interval for performing the steps [a through g in application] during steady state operation of the document processing system is about two seconds [col.4, ll.37-41; with Q=0 and ignoring calculation time assumed to be insignificant, focus on the more significant transmission time if that be the case so that the algorithm involving Q, V, and T would yield 2].

4.32. Cheung teaches that the advantage of using the round trip clock synchronization scheme as taught by Cristian can provide further precision tuning [col.3, ll.23-31] and enhance the accuracy of the network synchronization results [col.2, ll.47-52].

4.33. Shinoda et al., U.S. Patent 6675249, hereinafter Shinoda, discloses an information processing system with a processor for determining the compatibility of a plurality of clocks [col.7, ll.49-50].

4.34. Lackman et al., U.S. Patent 6343351, hereinafter Lackman, discloses a data processing system providing hard real-time service [col.3, ll.24-32].

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4.35. Lackman teaches the advantage of providing hard real-time service is the prevention of catastrophic results in critical systems due to data loss [col.3, ll.29-32].

4.36. Einbinder et al., U.S. Patent 6704302, hereinafter Einbinder, discloses a 10 base T network for connecting workstations [col.3, ll.4-19].

4.37. Kurd et al., U.S. Patent 6320424, hereinafter Kurd, discloses the synchronization of a clock during steady state operation [col.8, ll.10-12; col.9, ll.20-24].

4.38. Miyawaki, U.S. Patent 5995771, discloses a document processing system [image forming administration system] [fig.1].

4.39. Miyawaki discloses the system comprising a marking engine that marks a sheet to form at least a portion of a document [copier], the marking engine including a controller [control unit] [col.3, ll.54-63].

4.40. Miyawaki discloses the system comprising a resource that transfers the sheet to the marking engine [feeder] or receives the sheet from the marking engine [finisher] [col.4, ll.8-11].

4.41. Miyawaki discloses the system comprising a control bus [system bus 18], interconnecting the resource and the controller [col.4, ll.8-11, ll.35-39].

5. Yamanaka, Cheung, Shinoda, Lackman, Eibinder, and Kurd were cited as prior art in the previous Office Action.

Re Claim 1, 3, 6-7, 10-11, and 21

6. Claims 1, 3, 6-7, 10-11, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki in view of Yamanaka.

7. In re claim 1, Miyawaki discloses each and every limitation of the claim [findings 4.38-4.41].

Miyawaki did not discuss the details of synchronization between the controller of the marking engine and the resource. Yamanaka discloses a system comprising a controller, resource, and control bus with the synchronization details [findings 4.1-4.4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the synchronization teachings of Yamanaka into the document processing system of Miyawaki in order to synchronize operations among the resources and controller of the marking engine. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use [finding 4.18].

8. As to claim 3, see finding 4.5.
9. As to claim 6, see findings 4.6 and 4.7.
10. As to claim 7, see finding 4.8.
11. As to claim 10, see finding 4.11.
12. As to claim 11, see finding 4.12.
13. As to claim 21, see findings 4.2, 4.9 and 4.10.

Re Claim 2

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claim 1 above, and further in view of Shimoda.
15. In re claim 2, Yamanaka and Miyawaki disclose each and every limitation of the claim, as discussed above in reference to claim 1. Yamanaka and Miyawaki did not discuss the use of the resource processor for determining the compatibility of the slave clock with the master clock. Shimoda teaches a processor for determining the compatibility of a plurality of clocks [finding 4.33] in order to provide synchronization. It would have been obvious to one of ordinary skill in

the art at the time the invention was made to use the processor taught by Shimoda for determining the compatibility of the slave clock with the master clock in the resource circuitry disclosed by Yamanaka and Miyawaki as the processor taught by Shimoda is a known device for use in determining the compatibility between two values suitable for use as the processor of Yamanaka and Miyawaki. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for determining the compatibility between the two clocks for synchronization.

Re Claims 4 and 8

16. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claims 3 and 7 above, and further in view of Lackman.

17. In re claim 4, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 3. Miyawaki and Yamanaka did not discuss the use of the compatibility between the resource and the controller to provide hard real-time service. Lackman teaches a data processing system providing hard real-time service [finding 4.34] to avoid catastrophic results due to data loss within a limited time frame [finding 4.35]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Lackman before him at the time the invention was made, to modify the clock synchronization system disclosed by Miyawaki and Yamanaka to include the hard real-time service as taught by Lackman, in order to provide a hard real-time clock synchronization system [e.g., information from CPU 10 to CPU 20 must be received in a “fresh” state of no older than an X amount of clock cycles in order for system to function properly]. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for

ensuring the safety of the system with critical operations that need to be serviced within a limited time frame.

18. As to claim 8, see finding 4.13 and discussion above in reference to claim 4.

Re Claim 12

19. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claim 6 above, and further in view of Einbinder.

20. In re claim 12, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 6. Miyawaki and Yamanaka did not disclose expressly the use of a 10 base T network for interconnecting the resources and the controller. Einbinder teaches a 10 base T network for interconnecting nodes in a network to take advantage of the timing margins [finding 4.36]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 10 base T network as taught by Einbinder to connect the resources and controller disclosed by Miyawaki and Yamanaka as the 10 base T taught by Einbinder is a known connecting device for use in the system of Miyawaki and Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for interconnecting the resources and controller with controllable timing margins for synchronization purposes.

Re Claims 5, 9, and 13-20

21. Claims 5, 9, and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claims 1, 3, and 7 above, and further in view of Cheung.

22. In re claim 5, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 3. Miyawaki and Yamanaka did not discuss the detail of

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the compatibility between the resource and the controller to be such that the slave clock is synchronized to within one clock cycle of the master clock. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19], wherein the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [finding 4.21] in order to avoid problems for practical use [finding 4.18]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miyawaki and Yamanaka to include the synchronization mechanism as taught by Cheung, in order to obtain the compatibility between the resource and the controller such that the slave clock is synchronized to within one clock cycle of the master clock. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to synchronize the clocks within a range and avoid problems for practical use.

23. As to claim 9, see finding 4.13 and discussion above in reference to claim 5.

24. In re claim 13, Miyawaki and Yamanaka disclose each and every limitation of the claim as discussed above in reference to claim 1 [include findings 4.2-4.4 and 4.13-4.17]. Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19]. Thus, Cheung teaches a system similar to that of Miyawaki and Yamanaka. Cheung further teaches the steps the resource may take to synchronize its clock with the controller's master clock [findings 4.22-4.29] in order to increase the accuracy of the synchronization [finding 4.32]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miyawaki and Yamanaka to

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include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

25. As to claim 14, see finding 4.13 and discussion above in reference to claim 13.

26. In re claim 15, Miyawaki and Yamanaka discloses each and every limitation of the claim [findings 4.2-4.4 and 4.13-4.17]. Miyawaki and Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19]. Thus, Cheung teaches a system similar to that of Miyawaki and Yamanaka. Cheung further teaches the steps the resource may take to synchronize its clock with the controller's master clock [findings 4.22-4.26 and 4.30] in order to increase the accuracy of the synchronization [finding 4.32]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miyawaki and Yamanaka to include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

27. As to claim 16, see discussion above in reference to claim 5.

28. As to claim 17, see finding 4.37.

29. As to claim 18, see finding 4.31.

30. As to claim 19, see discussion above in reference to claim 14.

31. As to claim 20, see discussion above in reference to claim 9.

Response to Arguments

32. All rejections of claim limitations as filed prior to Amendment dated September 13, 2004 not argued substantively in response filed as said Amendment have been conceded by Applicant.

33. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various document processing systems.

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

36. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
November 22, 2004


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